UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,573	02/05/2004	Luke J. Mawst	032026-0754	2253

23524 7590 02/09/2006

FOLEY & LARDNER LLP
150 EAST GILMAN STREET
P.O. BOX 1497
MADISON, WI 53701-1497

EXAMINER	
DICKEY, THOMAS L	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 02/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/772,573	MAWST ET AL.
	Examiner	Art Unit
	Thomas L. Dickey	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21,23-29,32,34-46,48-52,54-56,59 and 63-67* is/are rejected.

7)☒ Claim(s) *22,30,31,33,47,53,57,58 and 60-62* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 12/19/05 has been entered.

Initially, it is noted that applicant added claims 66 and 67 without supplying reasons why said claims are patentable over the art of record, in violation of 37 CFR 1.111. However, no harm seems to have accrued. Applicants do argue the patentability of claims 1 and 39, from which the new claims depend. Further, it is clear that the new claims read on the same art as do claims 2 and 41, respectively.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. J S Harris Jr, "GaInNAs long-wavelength lasers: progress and challenges," Semicond. Sci. Technol. 17 (2002) pp 1–12. In section 2 and figure 2 Harris Jr. supplies facts refuting Applicant's argument, found at pp. 12-13 and repeated page 16 of the paper filed 12/19/05, that one of skill in the art would lack the technical know-how to lattice match alloys of indium, gallium, arsenic, and nitrogen to an InP substrate, while adjusting the band gap of the resultant alloy. The examiner found Harris Jr on the Web after a two minute Google search. If Applicant had any technical skill in the art of III-V alloys (or were willing to spend a few minutes making herself aware of the state of said art), Applicant would understand how ludicrous her position is. For the last ten years, every writer in this field has either spent a few paragraphs explaining lattice matching, as Harris Jr. does, or simply assumed their reader knew all about it, as

applicants do in their own specification. If there were any truth to Applicant's ludicrous suggestion – which there is not – her own claims would lack enablement.

New art has been applied to some of Applicant's claims. Consequently this action is Non-Final.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1,2,8,11,12,15, 16,17,18-21,23,24,25,26, 27,29,32,34,38, 39,48,49,52, 54, 59, and 63 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-33 of U.S. Patent No. 6,791,104 in view of PETER ET AL. ("Light-emitting diodes and laser diodes based on a $Ga_{1-x}In_xAs/GaAs_{1-y}Sb_y$" Applied Physics Letters, 04/05/99, Vol. 74 Issue 14, pp1951-1953).

With regard to claims 1,2,8,11,12,15,53, and 54, claims 1-33 of Patent No. 6,791,104 disclose an optoelectronic device comprising a multilayer semiconductor structure including a substrate and an active region, the active region comprising at least a hole quantum well layer of a semiconductor containing antimony and at least one electron quantum well layer adjacent to the hole quantum well layer which comprises a semiconductor containing nitrogen to provide a type II quantum well structure, wherein the semiconductor containing antimony is InGaAsSb and the semiconductor containing nitrogen is InAsN, wherein the semiconductor containing antimony is GaAsSb or InGaAsSb and the semiconductor containing nitrogen is InAsN or InGaAsN, wherein the electron quantum well layers and hole quantum well layer form a first quantum well stage, and wherein the active region comprises a plurality of quantum well stages adjacent to each other each having electron quantum well layers

surrounding a hole quantum well layer, including means for providing optical feedback to form an edge-emitting laser or a vertical cavity surface-emitting laser.

Claims 1-33 do not disclose that the substrate is an InP substrate. However, Peter et al. discloses an optoelectronic device with an InP substrate. Note the first column of page 1951 of Peter et al. Peter et al. explain that the binary InP substrate is advantageous in that it is commercially used and thus technically advanced, has good thermal conductivity and low electrical resistance. Therefore, it would have been obvious to a person having skill in the art to replace the substrate of the device of claims 1-33 with the InP substrate such as taught by Peter et al. in order to provide a substrate that is technically advanced, has good thermal conductivity and low electrical resistance to thus provide higher reliability.

With regard to claims 16,17,18-21,23,24,25,26, and 59, claims 1-33 of Patent No. 6,791,104 disclose an optoelectronic device comprising a multilayer semiconductor structure including a substrate and an active region, the active region comprising at least a hole quantum well layer of GaAsSb or InGaAsSb and an electron quantum well layer of InAsN or InGaAsN on each side of the hole quantum well layer to provide a type II quantum well structure, wherein the electron quantum well layers are in compressive strain and the hole quantum well layer is in compressive strain and the thickness of each electron quantum well layer and hole quantum well layer is between approximately 10 and 50 angstroms, wherein the electron quantum well layers and hole quantum well

layer form a first quantum well stage, and wherein the active region comprises a plurality of quantum well stages adjacent to each other and the electron quantum well layer is an InAsN layer, wherein the hole quantum well layer is an InGaAsSb layer and the electron quantum well layer is an InAsN layer, and including means for providing optical feedback to form an edge-emitting laser or a vertical cavity surface-emitting laser.

Claims 1-33 do not disclose that the substrate is an InP substrate. However, Peter et al. discloses an optoelectronic device with an InP substrate. Note the first column of page 1951 of Peter et al. Peter et al. explain that the binary InP substrate is advantageous in that it is commercially used and thus technically advanced, has good thermal conductivity and low electrical resistance. Therefore, it would have been obvious to a person having skill in the art to replace the substrate of the device of claims 1-33 with the InP substrate such as taught by Peter et al. in order to provide a substrate that is technically advanced, has good thermal conductivity and low electrical resistance to thus provide higher reliability.

With regard to claims 27,29,32,34, and 38, claims 1-33 of Patent No. 6,791,104 disclose an optoelectronic device comprising a multilayer semiconductor structure including a substrate and an active region, the active region comprising at least a hole quantum well layer of GaAsSb and an electron quantum well layer of InAsN on each side of the hole quantum well layer to provide a type II quantum well structure wherein

the electron quantum well layers are in compressive strain and the hole quantum well layer is in compressive strain, wherein the thickness of each electron quantum well layer and hole quantum well layer is between approximately 10 and 50 angstroms, wherein the electron quantum well layers and hole quantum well layer form a first quantum well stage, and wherein the active region comprises a plurality of quantum well stages adjacent to each other, and including means for providing optical feedback to form an edge-emitting laser or a vertical cavity surface-emitting laser.

Claims 1-33 do not disclose that the substrate is an InP substrate. However, Peter et al. discloses an optoelectronic device with an InP substrate. Note the first column of page 1951 of Peter et al. Peter et al. explain that the binary InP substrate is advantageous in that it is commercially used and thus technically advanced, has good thermal conductivity and low electrical resistance. Therefore, it would have been obvious to a person having skill in the art to replace the substrate of the device of claims 1-33 with the InP substrate such as taught by Peter et al. in order to provide a substrate that is technically advanced, has good thermal conductivity and low electrical resistance to thus provide higher reliability.

With regard to claims 39,48,49,52,62 and 63, claims 1-33 of Patent No. 6,791,104 disclose an semiconductor laser comprising (a) a multilayer semiconductor structure including a substrate and an active region, the active region comprising at least a hole quantum well layer of a semiconductor containing antimony and at least one electron

quantum well layer comprising a semiconductor containing nitrogen adjacent to the hole quantum well layer to provide a type II quantum well structure; and (b) means for providing optical feedback to provide lasing action in the active region, wherein the means for providing optical feedback forms an edge-emitting laser or a vertical cavity surface-emitting laser, wherein the semiconductor containing antimony is InGaAsSb the semiconductor containing nitrogen is InAsN.

Claims 1-33 do not disclose that the substrate is an InP substrate. However, Peter et al. discloses an optoelectronic device with an InP substrate. Note the first column of page 1951 of Peter et al. Peter et al. explain that the binary InP substrate is advantageous in that it is commercially used and thus technically advanced, has good thermal conductivity and low electrical resistance. Therefore, it would have been obvious to a person having skill in the art to replace the substrate of the device of claims 1-33 with the InP substrate such as taught by Peter et al. in order to provide a substrate that is technically advanced, has good thermal conductivity and low electrical resistance to thus provide higher reliability.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

> invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 1,2,5,8,11-16,18,21,24,25,26,27,28,29,32,34-41,43-46,48-51,54,59, and 63-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over PETER ET AL. ("Light-emitting diodes and laser diodes based on a $Ga_{1-x}In_xAs/GaAs_{1-y}Sb_y$" Applied Physics Letters, 04/05/99, Vol. 74 Issue 14, pp1951-1953), in view of Major et al. (5,689,123).

With regard to claims 1,2,8, 11-14, 54, and 66 Peter et al. disclose a multilayer semiconductor structure including an InP substrate and an active region, the active region comprising at least a hole quantum well layer of a semiconductor containing antimony and at least one electron quantum well layer adjacent to the hole quantum well layer which comprises a first semiconductor to provide a type II quantum well structure, wherein the first semiconductor comprises InAs, the semiconductor containing antimony is GaAsSb or InGaAsSb and the first semiconductor comprises InAs or InGaAs, the electron quantum well layers are in compressive strain and the hole quantum well layer are in tensile strain, the electron quantum well layers and hole quantum well layer form a first quantum well stage, and wherein the active region comprises a plurality of quantum well stages adjacent to each other each having electron quantum well layers surrounding a hole quantum well layer, and the active region generates light including means for providing optical feedback to form an edge-emitting laser or a vertical cavity surface-emitting laser.

With further regard to claims 39,40,41,43-46,48-51, 63-65, and 67 Peter et al. disclose a semiconductor laser including (a) an InP substrate and an active region, the active region comprising at least a hole quantum well layer of a semiconductor containing antimony and at least one electron quantum well layer comprising a first semiconductor adjacent to the hole quantum well layer to provide a type II quantum well structure; wherein there is an electron quantum well layer on each side of the hole quantum well layer and there is a barrier layer adjacent to each electron quantum well layer on each side of the hole quantum well layer to provide a conduction band profile for the active region having a W-shaped configuration, the semiconductor containing antimony is GaAsSb or InGaAsSb and the first semiconductor comprises InAs or InGaAs, wherein the electron quantum well layers are in compressive strain and the hole quantum well layer is in tensile strain, the thickness of each electron quantum well layer and hole quantum well layer is between approximately 10 and 50 angstroms, the electron quantum well layers and hole quantum well layer form a first quantum well stage, and wherein the active region comprises a plurality of quantum well stages adjacent to each other each having electron quantum well layers surrounding a hole quantum well layer, the first semiconductor comprises InAs, and wherein there is an optical confinement layer adjacent to each barrier layer, the optical confinement layer comprising InP, and (b) means for providing optical feedback to provide lasing action in

the active region, the means for providing optical feedback forming an edge-emitting laser or a vertical cavity surface-emitting laser.

With regard to any of the above listed claims (1,2,5,8, 11-14, 54, and 66, 39,40,41,43-46,48-51, 63-65, and 67) the only difference between said claims and the device disclosed by Peter et al. is that Peter et al. does not disclose that the first semiconductor comprising InAs is a semiconductor containing nitrogen, in fact comprising InAsN, or that the active region generates light having a wavelength greater than approximately 2 microns or approximately 3 microns. In her paper filed 12/19/05, Applicant admits that these are the only differences.

However, Major et al. discloses a semiconductor laser with an electron quantum well layer comprising InAsN. Note figures 3-7 and column 11 lines 3-18 of Major et al. Major et al. teaches that adding as little as 4% nitrogen to $In_{.75}Ga_{.25}As$ (lattice matched to InP) while making minor adjustments to the In/Ga ratio to retain lattice match, produces a layer, with a band gap of .53 ev or less, which lases at 2-3 microns, making it useful for LIDAR systems. Furthermore, according to Major et al., strain on such a layer is reduced by the introduction of nitrogen, further reducing the effective laser wavelength. Therefore, it would have been obvious to a person having skill in the art to replace the InAs of the first semiconductor of Peter et al.'s semiconductor laser with the InAsN such as taught by Major et al. in order to reduce band gap and strain, increasing effective

laser wavelength to thus provide a laser capable of lasing at 2-3 microns, effective for LIDAR applications.

With regard to claims 16,18,20,21,24,25,26, and 59 Peter et al. disclose a multilayer semiconductor structure including an InP substrate and an active region, the active region comprising at least a hole quantum well layer of GaAsSb or InGaAsSb and an electron quantum well layer comprising InAs or InGaAs on each side of the hole quantum well layer to provide a type II quantum well structure, wherein the electron quantum well layer comprises a InAs layer, the thickness of each electron quantum well layer and hole quantum well layer is between approximately 10 and 50 angstroms, the electron quantum well layers and hole quantum well layer form a first quantum well stage, and wherein the active region comprises a plurality of quantum well stages adjacent to each other, and including means for providing optical feedback to form an edge-emitting laser or a vertical cavity surface-emitting laser.

With regard to claims 27,28,29,32, and 34-38 Peter et al. disclose a multilayer semiconductor structure including an InP substrate and an active region, the active region comprising at least a hole quantum well layer of GaAsSb and an electron quantum well layer comprising InAs on each side of the hole quantum well layer to provide a type II quantum well structure wherein (at least one of) the electron quantum well layers is lattice matched to InP, the thickness of each electron quantum well layer and hole quantum well layer is between approximately 10 and 50 angstroms, the

electron quantum well layers and hole quantum well layer form a first quantum well stage, and wherein the active region comprises a plurality of quantum well stages adjacent to each other, and including means for providing optical feedback to form an edge-emitting laser or a vertical cavity surface-emitting laser.

With regard to any of the above listed claims (16,18,20,21,24,25,26, and 59, 27,28,29,32, and 34-38) the only difference between said claims and the device disclosed by Peter et al. is that Peter et al. does not disclose that the electron quantum well layer comprising InAs further comprises nitrogen so that it comprises InAsN. In her paper filed 12/19/05, Applicant admits that this is the only difference.

However, Major et al. discloses a semiconductor laser with an electron quantum well layer comprising InAsN. Note figures 3-7 and column 11 lines 3-18 of Major et al. Major et al. teaches that adding as little as 4% nitrogen to $In_{.75}Ga_{.25}As$ (which is the InGaAs alloy, comprising InAs, that is lattice matched to InP) while making minor adjustments to the In/Ga ratio to retain lattice match, produces a layer with a band gap of .53 ev or less, which lases at 2-3 microns, making it useful for LIDAR systems. Furthermore, according to Major et al., strain on such a layer is reduced by the introduction of nitrogen, further reducing the effective laser wavelength. Therefore, it would have been obvious to a person having skill in the art to replace the InAs of the first semiconductor of Peter et al.'s semiconductor laser with the InAsN such as taught by Major et al. in

order to reduce band gap and strain, increasing effective laser wavelength to thus provide a laser capable of lasing at 2-3 microns, effective for LIDAR application.

B. Claims 1,3-10, 55, and 56 stand rejected under 35 U.S.C. 103(a) as being unpatentable over DAPKUS (6,621,842) in view of PETER ET AL. ("Light-emitting diodes and laser diodes based on a $Ga_{1-x}In_xAs/GaAs_{1-y}Sb_y$" Applied Physics Letters, 04/05/99, Vol. 74 Issue 14, pp1951-1953).

With regard to claims 1,3-7, 55, and 56 Dapkus discloses an optoelectronic device comprising a multilayer semiconductor structure including an substrate and an active region, the active region comprising at least a hole quantum well layer of a semiconductor containing antimony and at least one electron quantum well layer adjacent to the hole quantum well layer which comprises a semiconductor containing nitrogen to provide a type II quantum well structure, wherein the semiconductor containing antimony is GaAsSb or InGaAsSb, there is an electron quantum well layer on each side of the hole quantum well layer and there is a GaInP barrier layer adjacent to each electron quantum well layer on each side of the hole quantum well layer to provide a conduction band profile for the active region having a W-shaped configuration. Note figures 2-4, column 5 lines 1-67, column 6 lines 1-67, and column 7 lines 1-29 of Dapkus.

Dapkus does not disclose that the substrate is an InP substrate. However, Peter et al. discloses an optoelectronic device with an InP substrate. Note the first column of

page 1951 of Peter et al. Peter et al. explain that the binary InP substrate is advantageous in that it is commercially used and thus technically advanced, has good thermal conductivity and low electrical resistance. Therefore, it would have been obvious to a person having skill in the art to replace the substrate of the device of Dapkus with the InP substrate such as taught by Peter et al. in order to provide a substrate that is technically advanced, has good thermal conductivity and low electrical resistance to thus provide higher reliability.

With regard to claims 1,8,9, and 10 Dapkus discloses an optoelectronic device comprising a multilayer semiconductor structure including an substrate and an active region, the active region comprising at least a hole quantum well layer of a semiconductor containing antimony and at least one electron quantum well layer adjacent to the hole quantum well layer which comprises a semiconductor containing nitrogen to provide a type II quantum well structure, wherein the electron quantum well layers and hole quantum well layer form a first quantum well stage, and wherein the active region comprises a plurality of quantum well stages adjacent to each other each having electron quantum well layers surrounding a hole quantum well layer, and including a GaInP barrier layer between each quantum well stage to provide a conduction band profile having a W-shaped configuration. Note figures 2-4, column 5 lines 1-67, column 6 lines 1-67, and column 7 lines 1-29 of Dapkus.

Dapkus does not disclose that the substrate is an InP substrate. However, Peter et al. discloses an optoelectronic device with an InP substrate. Note the first column of page 1951 of Peter et al. Peter et al. explain that the binary InP substrate is advantageous in that it is commercially used and thus technically advanced, has good thermal conductivity and low electrical resistance. Therefore, it would have been obvious to a person having skill in the art to replace the substrate of the device of Dapkus with the InP substrate such as taught by Peter et al. in order to provide a substrate that is technically advanced, has good thermal conductivity and low electrical resistance to thus provide higher reliability.

Allowable Subject Matter

4. Claims 22,30,31,33,47,53,57,58, and 60-62 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

5. Applicant's arguments with respect to claims 1,2,8,11-16,18,21,24,25,26,27,28, 29,32, 34-41,43-46,48-51,54,59, and 63-67 have been considered but are moot in view of the new ground(s) of rejection.

It is argued, at page 11 of the remarks, that "The cited text provides no suggestion that an InP substrate is more desirable than a GaAs substrate." This argument is based on a misconception of the law of motivation. A finding that the prior art as a whole suggests the desirability of particular combination need only show exactly that: the desirability of that particular combination. In this case the desirability of the combination of the device disclosed by claims 1-33 of Patent No. 6,791,104 with an InP substrate is amply supported by the facts that InP is commercially used and thus technically advanced, has good thermal conductivity and low electrical resistance. There is no requirement of a finding that InP is "the preferred [i.e. "more desirable"], or most desirable combination." In re Fulton, 73 USPQ2d 1141, 1145 (Fed. Cir 2004) ("our case law does not require that a particular combination must be the preferred, or the most desirable, combination described in the prior art in order to provide motivation for the current invention").

It is argued, at page 12 of the remarks, that "Due to the complicated interplay between the substrate and the overlying layers in a multilayered optoelectronic device, one of ordinary skill in the art would not reasonably expect that replacing the GaAs substrate of the device described in the [claims 1-33] of the '104 Patent with the InP substrate of Peter et al. would provide a functioning optoelectronic device... [because] a paramount concern in fabricating a functioning optoelectronic device is the lattice match between the substrate and the overlying layers ... [and] its emission wavelength range."

If it were in fact true that one of ordinary skill in the art, having at his/her disposal all of the accumulated knowledge of the art, could not producing a functioning optoelectronic device having the limitations of any one of applicant's claims, that claim would fail the enablement requirements of section 112. In their specification, applicants do not bother to teach the details of creating the proper interplay of "lattice match between the substrate and the overlying layers ... [and] its emission wavelength range." Applicants don't teach this because they know (or at least at the time of filing they knew) that such knowledge was well within the skill of one having ordinary skill in the art. Besides, it is clear that Harris Jr taught such skills in 2002. For that matter, so did Major et al. 5,689,123, cited above, in 1997.

It is argued, at page 13 of the remarks, that "Regarding Claims 27, 54, 59 and 63, the Office Action asserts that the '104 Patent teaches a Type 11 quantum well structure, wherein the semiconductor containing nitrogen is [i.e., comprises] InAsN. However, the Office Action fails to cite (and applicants were unable to identify), any language in the '104 Patent that teaches or suggests the use of InAsN as an electron quantum well layer in a Type 11 quantum well structure." The office action specifically cited claims 1-33. Claim 16 of the cited claims 1-33 states, in relevant part, "electron quantum well layers adjacent to the hole quantum well layer at least one of which comprises InGaAsN to provide a type II quantum well structure," The electron quantum well layer of the type II quantum well structure of claim 16's electron quantum well layers thus comprise

InGaAsN, which comprises InAsN. Does applicant wish in response to assert that claim 27, 54, 59 and 63's InAsN layers are gallium free? Before doing so Applicant should re-examine figure 2 of Harris Jr. The band gap of gallium-free InAsN goes negative (optically inactive, metallic) at a lattice constant of 5.96 angstroms, well above the lattice constant of InP. Accord, figures 5 and 7 of Major et al. In view of Applicant's assertion that a non-lattice matched device cannot "reasonably" be expected to "provide a functioning optoelectronic device," it would appear that a claim to a device comprising an electron quantum well layer consisting of gallium-free InAsN is a claim to a device that cannot reasonably be expected to function for its intended purpose.

It is argued, at page 13 of the remarks, that claims 1-33 of 6,791,104 lack the InGaAsSb limitation of claims 53,58, and 62. Applicant's argument has merit and the double patenting rejection of claims 53,58, and 62 is withdrawn.

It is argued, at page 14 of the remarks, that "Peter. et al. does not teach or suggest a Type II quantum well structure that includes electron quantum well lavers comprising InAsN, InGaAsN, or any other nitrogen-containing semiconductor. Therefore, Peter, et al. fails to teach each and every limitation of [claims 1,2,8,11-16,18,21,24,25,26,27,28, 29,32, 34-41,43-46,48-51,54,59, and 63-65]." Applicant's argument has merit and the 102(b) rejection of claims 1,2,8,11-16,18,21,24,25,26,27,28,29,32,34-41,43-46,48-51,54,59, and 63-65 has been withdrawn.

It is argued, at page 14 of the remarks, that Peter et al. fails to disclose lasers having light-emitting regions capable of emitting light at 2-3 microns, as required by claims 50 and 51. This statement is, simply put, not true. Peter et al. reported seeing type II light emission at 2-3 microns and verified lasing (a subset of the group consisting of all light emission) at 1.71. Note page 1953, right hand column. Nonetheless, the 102(b) rejection of claims 50 and 51 is withdrawn, for other reasons.

It is argued with regard to claims 17 and 42 at page 15 of the remarks, that while Peter et al. admittedly (according to Applicant) discloses electron quantum well layers in compression and hole quantum well layers in tension, Peter et al. fails to disclose a device where both electron and hole quantum well layers are in compression. Applicant's argument has merit and the 102(b) rejection of claims 17 and 42 is withdrawn.

It is argued, at page 16 of the remarks, that "Peter et al. provides no motivation to replace the GaAs substrate described in Dapkus with the InP substrate of Peter et al." Assuming Applicant relies on the argument of page 11 for reasoning concerning the relative desirability of GaAs and InP substrates, this argument is based on two misconceptions of the law of motivation. Firstly, it is not Peter et al. that provides or fails to provide the motivation to combine or not; it is the prior art as a whole. Peter et al. is relied on for what it teaches, suggests, or implies about the state of the prior art as a whole. See In re Winslow, 151 USPQ 48,51 (CCPA, 1966)("Section 103 requires us to

presume full knowledge by the inventor of the *prior* art in the field of his endeavor.") Secondly, as stated before, a finding that the prior art as a whole suggests the desirability of particular combination need only show exactly that: the desirability of that particular combination. In this case the desirability of the combination of the device disclosed by Dapkus with an InP substrate is amply supported by the facts that InP is commercially used and thus technically advanced, has good thermal conductivity and low electrical resistance. There is no requirement of a finding that InP is the preferred [i.e. "more desirable"], or most desirable combination. In re Fulton, 73 USPQ2d 1141, 1145 (Fed. Cir 2004) ("our case law does not require that a particular combination must be the preferred, or the most desirable, combination described in the prior art in order to provide motivation for the current invention").

It is argued, at page 12 of the remarks, that "Dapkus and Peter et al. do not provide a reasonable expectation that the substitution of the GaAs substrate of Dapkus with the InP substrate of Peter et al. would provide a functioning optoelectronic device...As discussed in Section I ... in light of this complex relationship one of ordinary skill in the art [would be hopelessly confused and at a loss as to what to do]." If it were in fact true that one of ordinary skill in the art, having at his/her disposal all of the accumulated knowledge of the art, could not produc~~ing~~e a functioning optoelectronic device having the limitations of any one of applicant's claims, that claim would fail the enablement requirements of section 112. In their specification, applicants do not bother to teach the

details of creating the proper interplay of "lattice match between the substrate and the overlying layers ... [and] its emission wavelength range." Applicants don't teach this because they know (or at least at the time of filing they knew) that such knowledge was well within the skill of one having ordinary skill in the art. Besides, it is clear that Harris Jr taught such skills in 2002. For that matter, so did Major et al. 5,689,123 (cited above) in 1997.

It is argued, at page 17 of the remarks, that "Applicants further note that Dapkus fails to teach or suggest a semiconductor structure that includes an active region comprising an electron quantum well layer comprised of InAsN or InGaAsN, as recited in dependent Claims 2 and 54." This argument has merit and the 103(b) rejection of claims 2 and 54 over Dapkus in view of Peter et al. has been withdrawn.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thomas L. Dickey
Patent Examiner
Art Unit 2826
02/06